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EXAMINER
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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/034,734	LI ET AL.
	Examiner	Art Unit	
	Charles Chow	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>28 March 2005</u>.

2a) ☒ This action is **FINAL**.   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-26</u> is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☒ Claim(s) <u>15,16 and 18</u> is/are allowed.

6) ☒ Claim(s) <u>1-14,17 and 19-26</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All   b)☐ Some * c)☐ None of:

   1. ☐ Certified copies of the priority documents have been received.

   2. ☐ Certified copies of the priority documents have been received in Application No. _____.

   3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

Detailed Action

1. Applicant's election without traverse of claims 1-26 in the reply filed on 3/28/2005 (page 12)

is acknowledged.

2. Applicant has corrected the title. The objection to title has been removed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fagan (GB

2,229,333A) in view of Prentice et al. (US 6,763,228 B2).

Regarding **claim 1**, Fagan teaches an automatic gain control AGC apparatus (Fig. 1-2,

abstract), an analog variable gain amplifier AVGA (coarse gain control element 14 for

receiving analog signal with variable gain control G1, B, Fig. 1, page 6, lines 1-16), a digital

variable gain amplifier DVGA (element 17 for amplifying 12-bit digital signal from ADC 16,

Fig. 1, page 6, lines 23-30), coupled to an output of the analog variable gain amplifier AVGA

(the element 17 coupled to element 14 via 16 ADC, Fig. 1), and a gain controller (processor

15) adapted to measure a signal output from the DVGA (the processor 15 receives V' from

18' for estimate the DVGA 17 output at 12, page 7, lines 15-27), and to control the gains of

the analog and digital variable gain amplifiers (the processor 15 provides control b to ADVA

14 and control signal G2 to DVGA 17, page 7, line 28 to page 8, line 34).

Fagan fails to teach the AGC apparatus operable during direct conversion of RF signals.

Prentice et al. (Prentice) teaches these features [the zero intermediate frequency ZIF

transceiver 101 in Fig. 1, col. 7, lines 4-20, abstract], the gain control can be performed in

linear format, and also can be in any desired format, such as log format [col. 3, lines 30-35],

to upgrade the AGC for the ZIF transceiver. Therefore, it would have been obvious to one of

ordinary skill in the art at the time of invention to modify Fagan with Prentice's precision

AGC, in order to upgrade the AGC for handling the ZIF transceiver with precision AGC.

4. Claims 3, 6, 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruelke

(US 6,459,889 B1) in view of Prentice-'228 B2.

Regarding **claim 3**, Ruelke teach a method of operating an automatic gain control AGC loop

in combination with a DC loop (the AGC loop formed by 140, 122, 158; the DC loop

formed by 160, 162, 164 and 186,168,170, Fig. 1, abstract), selecting a particular DC

operating mode for the DC loop from among a plurality of possible DC operating modes,

operating the DC loop in the selected DC operating mode to correct for DC offset in a

desired signal (the DC operating modes in steps 344, 348, 352, Fig. 3B, for non-slotted

system mode, to initiate digital correction sequence to correct DC baseband offset, and the

DC operating mode in steps 384, 376, 378, 382, for the slotted system mode, to initiate a

binary search to correct baseband DC in step 378; the first DE offset correction sequence

for non-slotted protocol and the second DC offset correction sequence for slotted protocol in

col. 12, lines 31-55; the DC offset correction for slotted protocol and different strategies for

non-slotted protocol, in col. 5, lines 26-40), selecting a particular AGC operating mode for

the AGC loop from among a plurality of possible AGC operating modes based on the

selected DC operating mode and operating the AGC loop in the selected AGC operating

mode to provide variable gain for the desired signal (for the non-slotted protocol, the first DC

offset correction sequence comprises the presetting a DC offset correction and allowing an,

particular, AGC loop to respond while DC offset correction loop is correcting the DC offset,

and for the slotted protocol, the second DC offset correction sequence, setting the AGC to a

value which eliminates on-channel input signals and carrying out a Dc offset correction to

restore normal AGC operation in col. 12, lines 17-55; the AGC in steps 376-382 for slotted

protocol, the AGC in steps 344-352 for non-slotted protocol in Fig. 3B). Ruelke fails to teach

the AGC apparatus operable during direct conversion of RF signals. Prentice teaches these

features [the zero intermediate frequency ZIF transceiver 101 in Fig. 1, col. 7, lines 4-20,

abstract], the gain control can be performed in linear format, and also can be in any desired

format, such as log format [col. 3, lines 30-35], to upgrade the AGC for the ZIF transceiver.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of

invention to modify Ruelke with Prentice's precision AGC, in order to upgrade the AGC for

handling the ZIF transceiver with precision AGC.

Regarding **claim 6**, Ruelke teaches the plurality of possible AGC operating modes (signal

(the plurality of AGC operating modes for slotted and non-slotted environment and

protocols, abstract, col. 3, lines 31-53; col. 5, lines 26-54, Fig. 3B), is associated with a

respective AGC loop gain (the associated AGC loop gain setting in slotted protocol for 10 db

in step 376, and then reset AGC for nominal operation using fast AGC in step 382, Fig. 3B;

the associated AGC loop gain setting in the non-slotted protocol for initial condition IC in

step 344, and then simultaneous AGC setting while correcting DC offset in step 352).

Regarding **claim 11**, Ruelke teaches a receiver in a wireless communication system

(the receiver in abstract, Fig. 1, the Zif, DCR receiver in col. 3, lines 31-41, for AMPS, TDMA

system, col. 5,lines 42-55; col. 7, lines 62-67), comprising a DC loop configurable to operate

in one of a plurality of possible DC operating modes to correct for DC offset in a desired

signal (the both AGC and DC offset correction loop DOCL are dynamically configured for

optimum complimentary operation via microprocessor 236 and serial bus, Fig. 2, depending

on the receiver's operating environment and protocol, abstract; the plurality of DCOCL

operating modes for slotted protocol and non-slotted protocol, col. 3, lines 31-53; col. 5,

lines 26-54, Fig. 3B), and An AGC loop configurable to operate in one of a plurality of

possible AGC operating modes to variable gain for the desired signal (the plurality of AGC

operating modes for slotted and non-slotted environment and protocols, abstract, col. 3,

lines 31-53; col. 5, lines 26-54, Fig. 3B), wherein the particular AGC operating mode to be

used is determined based on the particular DC operating mode selected for use for the DC

loop (for the non-slotted protocol, the first DC offset correction sequence comprises the

presetting a DC offset correction and allowing an, selected particular, AGC loop to respond

while DC offset correction loop is correcting the DC offset, and for the slotted protocol, the

second DC offset correction sequence, setting the , selected particular, AGC to a value

which eliminates on-channel input signals and carrying out a DC offset correction to restore

normal AGC operation in col. 12, lines 17-55; the AGC in steps 376-382 for slotted protocol,

the AGC in steps 344-352 for non-slotted protocol in Fig. 3B). Ruelke fails to teach the

direction conversion receiver. Prentice teaches these features [the zero intermediate

frequency ZIF transceiver 101 in Fig. 1, col. 7, lines 4-20, abstract], the gain control can be

performed in linear format, and also can be in any desired format, such as log format [col.

3, lines 30-35], to upgrade the AGC for the ZIF transceiver. Therefore, it would have been

obvious to one of ordinary skill in the art at the time of invention to modify Ruelke with

Prentice's precision AGC, in order to upgrade the AGC for handling the ZIF transceiver with

precision AGC.

Regarding **claim 12**, Ruelke teaches an control apparatus (microprocessor 236, serial bus

242, Fig. 2) in a wireless communication system (the AMPS, TDMA system in col. 5, lines

42-55; col. 7, lines 62-67), comprising means for selecting a particular DC operating mode

for a DC loop from among a plurality of possible DC operating modes (the both AGC and DC

offset correction loop DOCL are dynamically configured for optimum complimentary

operation via microprocessor 236 and serial bus, Fig. 2, depending on the receiver's

operating environment and protocol, abstract; the plurality of DCOCL operating modes for

slotted protocol and non-slotted protocol, col. 3, lines 31-53; col. 5, lines 26-54, Fig. 3B),

means for operating the DC loop in the selected DC operating mode to correct for DC in the

desired signal (the DC operating modes in steps 344, 348, 352, Fig. 3B, for non-slotted

system mode, to initiate digital correction sequence to correct DC baseband offset, and the

DC operating mode in steps 384, 376, 378, 382, for the slotted system mode, to initiate a

binary search to correct baseband DC in step 378; the first DC offset correction sequence

for non-slotted protocol and the second DC offset correction sequence for slotted protocol in

col. 12, lines 31-55; the DC offset correction for slotted protocol and different strategies for

non-slotted protocol, in col. 5, lines 26-40), means for selecting a particular AGC operating

mode for an AGC loop from among a plurality of possible AGC operating modes base on the

selected DC operating mode and means for operating AGC loop in the selected AGC

operating mode to provide variable gain for the desired signal (the plurality of AGC operating

modes for slotted and non-slotted environment and protocols, abstract, col. 3, lines 31-53;

col. 5, lines 26-54, Fig. 3B, the non-slotted protocol, the first DC offset correction sequence

comprises the presetting a DC offset correction and allowing an, selected particular, AGC

loop to respond while DC offset correction loop is correcting the DC offset, and for the

slotted protocol, the second DC offset correction sequence, setting the , selected particular,

AGC to a value which eliminates on-channel input signals and carrying out a DC offset

correction to restore normal AGC operation in col. 12, lines 17-55; the AGC in steps 376-

382 for slotted protocol, the AGC in steps 344-352 for non-slotted protocol in Fig. 3B).

Ruelke fails to teach the adapted for use in a direction conversion receiver. Prentice teaches these features [the zero intermediate frequency ZIF transceiver 101 in Fig. 1, col. 7, lines 4-20, abstract], the gain control can be performed in linear format, and also can be in any desired format, such as log format [col. 3, lines 30-35], to upgrade the AGC for the ZIF transceiver. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Ruelke with Prentice's precision AGC, in order to upgrade the AGC for handling the ZIF transceiver with precision AGC.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fagan in view of Prentice, as applied to claim 1 above, and further in view of Becker et al. (US 5,612,975) and Webster et al. (US 6,748,200 B1).

Regarding **claim 2**, Fagan, Prentice fail to teach a DC offset canceller interposed between the output of the analog variable gain amplifier AVGA and an digital variable gain amplifier DVGA. However, Becker et al. (Becker) teaches this features, the DC bias remover 235 between variable amplifier 206, the wide band AGC 280 and post detection AGC digital amplifier 248 (col. 9, lines 17-22, col. 9, line 61 to col. 10, line 20, Fig. 9, Fig. 13, col. 13, lines 36-62). Becker fails to teach the AGC loop gain varies according to the operating mode of the DC offset canceller. Webster teaches teach the AGC loop gain varies according to the operating mode of the DC offset canceller, the AGC/DC control 141 (Fig. 1) generate GC to adjust the gain for AVGA, BB-AGC 125, via 147, 151, and generating GDADJ for adjusting the DVGA 135 (col. 8, lines 29-36; col. 8, line 59 to col. 9, line 29), according to the DC offset input to 139 BB-DC offset and signal power estimate, the DCE output from 139 to 141 (col. 8, line 37 to col. 10, line 60). Webster teaches the AGC system having the DC control loop for the ZIF of a wireless communication device (col. 1, lines 20-27), for improving of the DC offset error in a short time associated with an AGC procedure (col. 2, lines 43-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of

invention to modify Fagan, Prentice, Becker with Becker's fast DC offset removal with AGC,

such that the DC offset could be quickly removed in the AGC loop for a wireless

communication device.

6. Claims 4-5, 13-14, 17, 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Ruelke in view of Prentice, as applied to claim 3 above, and further in view of Dutkiewicz et

al. (US 5,629,960).

Regarding **claim 4**, Ruelke, Prentice fails to teach the DC operating modes including an

acquisition mode and tracking mode. However, Dutkiewicz et al. (Dutkiewicz) teaches the

acquisition mode for DC offset correction by utilizing acquire input at DC tracking 23 (Fig. 3)

from control 26 (col. 3, lines 52-61, the acquire mode for rapid tracking, col. 5, lines 28-44),

the DC offset tracking mode input to DC tracking 23, the wider bandwidth in acquire mode

for quick synchronization, the narrow bandwidth for DC offset tracking mode to reduce noise

(col. 3, line 44 to col. 4, line 26), the large DC offset shift (col. 4, lines 50-58). Dutkiewicz

teaches reducing the distortion effect on the DC offset due to large transient, to improve the

symbol clock synchronization effect (col. 1, line 61 to col. 2, lines 46), by utilizing the wide

bandwidth acquisition mode and narrow bandwidth tracking mode. Therefore, it would have

been obvious to one of ordinary skill in the art at the time of invention to modify Ruelke,

Prentice with Dutkiewicz's acquisition mode and tracking mode, such that the receiver could

track the time information by removing the DC offset distortion.

Regarding **claim 5**, Dutkiewicz teaches the acquisition mode has a wider loop bandwidth

than that of the tracking mode, and is used to more quickly remove a large DC offset in the

desired signal (col. 3, line 44 to col. 4, line 26; the large DC offset shift (col. 4, lines 50-58).

Regarding **claim 13**, Ruelke teaches a method of operating DC loop in a receiver unit

(the DC operating loop for correcting DC offset in different protocol modes, for the slotted

and non-slotted protocol in Fig. 3B, and in col. 3, col. 5, col. 12; the ZIF, DCR receiver, col.

3, line 34-35), selecting a particular operating mode for the DC loop from among a plurality

of possible operating modes (the DC operating modes in steps 344, 348, 352, Fig. 3B, for

non-slotted system mode, to initiate digital correction sequence to correct DC baseband

offset, and the DC operating mode in steps 384, 376, 378, 382, for the slotted system

mode, to initiate a binary search to correct baseband DC in step 378; the first DE offset

correction sequence for non-slotted protocol and the second DC offset correction sequence

for slotted protocol in col. 12, lines 31-55; the DC offset correction for slotted protocol and

different strategies for non-slotted protocol, in col. 5, lines 26-40). Prentice teach the

direction conversion receiver [the zero intermediate frequency ZIF transceiver 101 in Fig. 1,

col. 7, lines 4-20, abstract]. Ruelke, Prentice fail to teach the operating the DC loop in the

selected acquisition mode for the particular time duration to correct for DC offset wherein the

particular time duration is inversely proportional to a loop bandwidth for the DC loop for the

acquisition mode. However, Dutkiewicz teaches the operating the DC loop in the selected

acquisition mode for the particular time duration to correct for DC offset wherein the

particular time duration (the particular time during acquire mode using wider DC offset loop

bandwidth for quick synchronization, col. 3, lines 56-61), the short time 10-20 milliseconds,

for the particular time duration is inversely proportional to a loop bandwidth (col. 5, lines 31-

32), the transitioning out of the acquisition mode after the particular time duration (the until a

short time after the Tx/off, typically 10-20 milliseconds, col. 5,l ines 28-32). Dutkiewicz

teaches reducing the distortion effect on the DC offset due to large transient, to improve the

symbol clock synchronization effect (col. 1, line 61 to col. 2, lines 46), by utilizing the wide

bandwidth acquisition mode and narrow bandwidth tracking mode, for the DC offset

correction loop. Therefore, it would have been obvious to one of ordinary skill in the art at

the time of invention to modify Ruelke, Prentice with Dutkiewicz's wide bandwidth acquisition

mode and narrow bandwidth tracking mode, such that the receiver could track the time

information by removing the DC offset distortion.

Regarding **claim 14**, Dutkiewicz teaches the acquisition mode is selected in response to an

event to result in a large DC offset in the desired signal (col. 3, line 53 to col. 4, line 26; col.

4, lines 50-58).

Regarding **claim 17**, Dutkiewicz teaches the possible tracking mode (42, 23, Fig. 3, col. 2,

lines 30-37; col. col. 3, lines 49-57).

Regarding **claim 19**, Dutkiewicz teaches the particular time duration is selected based on an

expected amplitude of the DC offset in the desired signal (the particular time just before key

on time and until a short time after the key off, col. 2, lines 30-37).

Regarding **claim 20**, Dutkiewicz teaches the particular time duration is further selected to

minimize a combination of DC offset introduced in the desired signal (the time duration for

wide bandwidth acquire mode for quick synchronization in col. 3, lines 57-61) and loop noise

from DC loop (the reducing nose on the tracking sub-system, col. 3, lines 53-57, for the time

duration for narrow band tracking mode)

Regarding **claim 21**, Ruelke teaches the DC loop in a receiver (receiver in abstract, col. 3,

lines 34-35, the DC loop 160,162,164, 186,168, 170, Fig. 1). Prentice teaches the user in

the direct conversion receiver [the zero intermediate frequency ZIF transceiver 101 in Fig.

1, col. 7, lines 4-20, abstract]. Ruelke, Prentice fail to teach a summer. However, Dutkiewicz

teaches a summer operative to subtract a DC offset value form the desired signal to provide

a DC offset corrected signal (22, Fig. 3, col. 3, line 32-37), a loop control unit (26)

configurable to operate in one of a plurality of possible operating modes to provide the DC

offset value (the plurality of operating modes, track, or acquire, to DC tracking 23, Fig. 3),

wherein the plurality of possible operating modes include the acquisition mode having

particular wide bandwidth (Fig. 3, col. col. 3, lines 44-61), wherein the loop control unit is

operated in the acquisition mode (the controller 26 has DC offset mode select 42, Fig. 3),

wherein the particular time duration (the particular time during acquire mode using wider DC

offset loop bandwidth for quick synchronization, col. 3, lines 56-61), the short time 10-20

milliseconds, for the particular time duration is inversely proportional to a loop bandwidth

(col. 5, lines 31-32), the transitioning out of the acquisition mode after the particular time

duration (the until a short time after the Tx/off, typically 10-20 milliseconds, col. 5, lines 28-

32). Dutkiewicz teaches reducing the distortion effect on the DC offset due to large transient,

to improve the symbol clock synchronization effect (col. 1, line 61 to col. 2, lines 46), by

utilizing the wide bandwidth acquisition mode and narrow bandwidth tracking mode, for the

DC offset correction loop. Therefore, it would have been obvious to one of ordinary skill in

the art at the time of invention to modify Ruelke, Prentice with Dutkiewicz's wide bandwidth

acquisition mode and narrow bandwidth tracking mode, such that the receiver could track

the time information by removing the DC offset distortion.

Regarding **claim 22**, Ruelke teaches an apparatus in receiver (the DCOCL in receiver in

abstract, col. 3, lines 34-35, the DC loop 160,162,164, 186,168, 170, Fig. 1). Ruelke teaches

means for selecting a particular operating mode for DC loop (steps in Fig. 3B, for the DC

operating modes for slotted protocol or non-slotted protocol). Prentice teaches the user in

the direct conversion receiver [the zero intermediate frequency ZIF transceiver 101 in Fig.

1, col. 7, lines 4-20, abstract]. Ruelke, Prentice fail to teach the acquisition mode and the

means for operating DC loop in the acquisition mode for a particular time duration, (Fig. 3,

col. col. 3, lines 44-61), wherein the loop control unit is operated in the acquisition mode (the

controller 26 has DC offset mode select 42, Fig. 3), wherein the particular time duration (the

particular time during acquire mode using wider DC offset loop bandwidth for quick

synchronization, col. 3, lines 56-61), the short time 10-20 milliseconds, for the particular time

duration is inversely proportional to a loop bandwidth (col. 5, lines 31-32), the transitioning

out of the acquisition mode after the particular time duration (the until a short time after the

Tx/off, typically 10-20 milliseconds, col. 5, lines 28-32). Dutkiewicz teaches reducing the

distortion effect on the DC offset due to large transient, to improve the symbol clock

synchronization effect (col. 1, line 61 to col. 2, lines 46), by utilizing the wide bandwidth

acquisition mode and narrow bandwidth tracking mode, for the DC offset correction loop.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of

invention to modify Ruelke, Prentice with Dutkiewicz's wide bandwidth acquisition mode and

narrow bandwidth tracking mode, such that the receiver could track the time information by

removing the DC offset distortion.

7. Claim 7 is are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruelke in view of

Prentice, as applied to claim 3 above, and further in view of Sutterlin et al. (US 5,463,662).

Regarding **claim 7,** Ruelke teaches the reset AGC for nominal operation using fast AGC

(step 382, Fig. 3B). Ruelke, Prentice fail to teach the low gain mode in the AGC operating

modes. However, Sutterlin et al. (Sutterlin) teaches the low gain mode in the AGC operating

modes (the AGC state diagram having the high gain state, Fig. 6, col. 12, lines 10-14; the

low gain state, Fig. 6, col. 12, lines 43-56; col. 11, lines 15-45), for reducing gain error due to

noise (col. 1, line 20 to col. 2, line 9). Ruelke suggest AGC control but not the low gain

mode. Sutterlin teaches the low gain mode for reducing the noise effect on the received

signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Ruelke, Prentice with Sutterlin's low gain state, such that the receiver could reduce the noise signal.

8. Claim 8 is are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruelke in view of Prentice, Sutterlin, as applied to claim 7 above, and further in view of Heck et al. (US 5,483,691).

Regarding **claim 8,** Ruelke, Prentice, Sutterlin fail to teach the freeze mode in AGC operating modes, although Sutterlin teaches the improved technique for better signal to noise ratio in the AGC system (col. 1, lines 26-50). However, Heck et al. (Heck) teaches the freeze mode for AGC operating mode, the limiting the gain reduction upon gain control signal reaching a predetermined gain reduction limit threshold, for providing improved signal to noise ratio (col. 1, line 59 to col. 2, line 4, abstract), for the freezing mode of the AGC operation at the gain limit threshold. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Ruelke, Prentince, Sutterlin with Heck's the limiting gain reducing at predetermined threshold, such that the receiver could provide the improved signal to noise ratio.

9. Claim 9 is are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruelke in view of Prentice, Dutkiewicz, as applied to 4 above, and further in view of Sutterlin-'662.

Regarding **claim 9,** Dutkiewicz teaches the acquire mode for the DC operating mode (42, DC tracking 23, Fig. 3). Ruelke teaches the AGC modes for slotted and non-slotted protocols. Ruelke, Prentice, Dutkiewicz faii to teach the selected AGC operating mode is a low gain mode when selected DC operating mode is the acquisition mode. However,

Sutterlin teaches the low gain mode for the AGC states in Fig. 6. for preventing the noise interference (col. 1, line 20 to col. 2, line 9). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Ruelke, Prentice, Dutkiewicz with Sutterlin's low gain state, such that such that the receiver could reduce the noise signal.

10. Claim 10 is are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruelke in view of Prentice, Dutkiewicz, as applied to claim 4 above, and further in view of Heck-'691. Regarding **claim 10** Dutkiewicz teaches the acquire mode for the DC operating mode (42, DC tracking 23, Fig. 3). Ruelke teaches the AGC modes for slotted and non-slotted protocols. Ruelke, Prentice, Dutkiewicz fail to teach the selected AGC operating mode is a freeze mode when selected DC operating mode is the acquisition mode. However, Heck teaches the freeze mode for AGC operating mode, the limiting the gain reduction upon gain control signal reaching a predetermined gain reduction limit threshold, for providing improved signal to noise ratio (col. 1, line 59 to col. 2, line 4, abstract), for the freezing mode of the AGC operation at the gain limit threshold. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Ruelke, Prentice, Dutkiewicz with Heck's the limiting gain reducing at predetermined threshold, such that the receiver could provide the improved signal to noise ratio.

11. Claims 23-24, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fagan in view of Prentice, and further in view of Kotzian (US 5,014,013). Regarding **claim 23,** Fagan teaches a method of digitally amplifying a desired signal (the fine gain control element 17 for digitally amplifying signal received from ADC 16, page 6, lines 23-30), receiving a gain represented in a logarithm format (the received G1, G2, in dBV

of the logarithm format, page 12, lines 4-21), determining a different between the received

gain and a gain offset (the received gain V' and desired output level 11 are compared for

difference in element 20 and sending gain error value to processor 15, Fig. 1, page 7, line

15 to page 8, line 35), digitally multiplying the desired signal with the output gain (the digital

multiplier in element 17, fine gain control, based on binary value of G2 from processor; the

multiplying N factor of the G1 in coarse gain control element 14, page 6, lines 1-30).

Prentice teaches the direct conversion receiver (above), the gain control can be performed

in linear format, and also can be in any desired format, such as log format [col. 3, lines 30-

35]. Fagan, Prentice fail to teach the converting the difference in logarithm format to an input

gain in linear format. However, Kotzian teaches this feature, the antilog 86 for converting

received gain error signal to linear gain value for linear amplifier 87, and adding gain in

logarithm value is to multiply gain in linear value (Fig. 2, col. 2, lines 37-66; col. 4, line 32 to

col. 5, line 2). Fagan has taught the digital gain control G1, G2 in dBV format, Fagan does

not clearly describe whether the G1, G2 gain values are applied to multiplier in logarithm or

linear format. Kotzian teaches the antilog circuit for converting the logarithm gain error value

to linear format so that the linear value can be conveniently, flexibly, applied to the audio,

video, where the linear gain values are needed (col. 1, line 60 tc col. 2, line 6). Therefore, it

would have been obvious to one of ordinary skill in the art at the time of invention to modify

Fagan with Kotzian's antilog circuits for converting logarithm gain value to linear gain value,

such that the amplifier gain could be corrected by utilizing the required linear gain value.

Regarding **claim 24**, Fagan teaches a method of digitally amplifying a desired signal (the

fine gain control element 17 for digitally amplifying signal received from ADC 16, page 6,

lines 23-30), receiving a gain represented in a logarithm format (the received G1, G2, in dBV

of the logarithm format, page 12, lines 4-21), determining a different between the received

gain and a gain offset (the received gain V' and desired output level 11 are compared for

difference in element 20 and sending gain error value to processor 15, Fig. 1, page 7, line

15 to page 8, line 35), digitally multiplying the desired signal with the output gain (the digital

multiplier in element 17, fine gain control, based on binary value of G2 from processor; the

multiplying N factor of the G1 in coarse gain control element 14, page 6, lines 1-30).

Prentice teach the direct conversion receiver (above). Fagan, Prentice fail to teach the

converting the difference in logarithm format to an input gain in linear format. However,

Kotzian teaches this feature, the antilog 86 for converting received gain error signal to linear

gain value for linear amplifier 87, and adding gain in logarithm value is to multiply gain in

linear value (Fig. 2, col. 2, lines 37-66; col. 4, line 32 to col. 5, line 2). Fagan has taught the

digital gain control G1, G2 in dBV format, Fagan does not clearly describe whether the G1,

G2 gain values are applied to multiplier in logarithm or linear format. Kotzian teaches the

antilog circuit for converting the logarithm gain error value to linear format so that the linear

value can be conveniently, flexibly, applied to the audio, video, where the linear gain values

are needed (col. 1, line 60 to col. 2, line 6). Therefore, it would have been obvious to one of

ordinary skill in the art at the time of invention to modify Fagan, Prentice with Kotzian's

antilog circuits for converting logarithm gain value to linear gain value, such that the

amplifier gain could be corrected by utilizing the required linear gain value.

Regarding **claim 26**, Fagan teaches a method of digitally amplifying a desired signal (the

fine gain control element 17 for digitally amplifying signal received from ADC 16, page 6,

lines 23-30), receiving a gain represented in a logarithm format (the received G1, G2, in dBV

of the logarithm format, page 12, lines 4-21), determining a different between the received

gain and a gain offset (the received gain V' and desired output level 11 are compared for

difference in element 20 and sending gain error value to processor 15, Fig. 1, page 7, line

15 to page 8, line 35), digitally multiplying the desired signal with the output gain (the digital

multiplier in element 17, fine gain control, based on binary value of G2 from processor; the

multiplying N factor of the G1 in coarse gain control element 14, page 6, lines 1-30).

Prentice teaches the for use in a direct conversion receiver (above). Fagan, Prentice fail to

teach the converting the difference in logarithm format to an input gain in linear format.

However, Kotzian teaches this feature, the antilog 86 for converting received gain error

signal to linear gain value for linear amplifier 87, and adding gain in logarithm value is to

multiply gain in linear value (Fig. 2, col. 2, lines 37-66; col. 4, line 32 to col. 5, line 2). Fagan

has taught the digital gain control G1, G2 in dBV format, Fagan does not clearly describe

whether the G1, G2 gain values are applied to multiplier in logarithm or linear format.

Kotzian teaches the antilog circuit for converting the logarithm gain error value to   linear

format so that the linear value can be conveniently, flexibly, applied to the audio, video,

where the linear gain values are needed (col. 1, line 60 to col. 2, line 6). Therefore, it would

have been obvious to one of ordinary skill in the art at the time of invention to modify Fagan,

Prentice with Kotzian's antilog circuits for converting logarithm gain value to linear gain

value, such that the amplifier gain could be corrected by utilizing the required linear gain

value.

12. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fagan in view of

Prentice, Kotzian, as applied to claim 24 above, and further in view of Wilson (US

5,627,857).

Regarding **claim 25,** Fagan, Prentice, Koztian fail to teach the multiplexer and wherein the

digital multiplier is operating to multiply in phase and quadrature phase input samples in a

time division multiplexed manner. However, Wilson teaches this features, the mux 305 for

multiplexing in phase I and quadrature Q signal (Fig. 3, col. 4, line 61 to col. 5, line 63),

having digital multiplier 405 for multiplying digital gain to the sampled I, Q, RSSI value (Fig.

4, col.5, lines 39-63) in time division multiplexed manner at 38.4 ksamples/ second (col. 5,

lines 1-26), which is equivalent to applicant's multiplier 316. Koztian teaches the digital AGC

with improved gain error by eliminating the nonlinear errors (col. 2, lines 32-64) and Fagan

has taught above the digital gain loop and digital multiplier. Therefore, it would have been

obvious to one of ordinary skill in the art at the time of invention to modify Fagan, Prentice,

Kotzian with Wilson's mux 305, multiplier 405, such that the gain for the AGC loop could be

adjusted with improved error by eliminating nonlinear error.

Allowable Subject Matter

13. The following is an examiner's statement of reasons for allowance:

Applicant has amended **claims 15-16, 18** to be the independent claims, with the claimed

features from the previously objected claims 15-16, 18, in the office action.

Claims 15-16, 18 are allowable over the prior art of record, the prior art fails to teach singly,

particularly, or in combination, the subject matter, for operating a AGC DC loop, the

selecting operating mode including acquisition mode; and if the selected operating mode is

the acquisition mode, operating the DC loop for a particular time duration to correct DC

offset, with the particular duration which is inversely proportional to a loop bandwidth for the

DC loop, and transitioning out the acquisition mode after the particular time duration, the

acquisition mode being selected in response to an event expected to the result in a large DC

offset in the desired signal. The cited prior arts in above, Fagan, Ruelke, Becker, Webster,

Dutkiewicz, Sutterlin, Heck, Kotzian,Wilson, fall to teach the above claimed features.

Other prior arts in below has been considered, but they fail to teach the above claimed

features.

Severson et al. (US 2003/0100,286, A1), in May, 2003, teaches the AGC loop 170, the DC

offset loop 140, (Fig. 1, abstract) for the direct conversion receiver. Severson et al. has later

filing date.

Any comments considered necessary by applicant must be submitted no later than the

payment of the issue fee and, to avoid processing delays, should preferably accompany the

issue fee. Such submissions should be clearly labeled "Comments on Statement of

Reasons for Allowance."

Response to Arguments

14. Applicant's arguments with respect to claims 1-14, 17, 19-26 have been considered but are

moot in view of the new ground(s) of rejection.

Regarding applicant's amendment based on the no teachings from the newly added

features, <u>direct conversion of RF signal,</u> the <u>gain signal from logarithmic format to linear</u>

<u>format</u> (applicant's amendment pages 14-15), the ground of rejection has been changed to

include Prentice et al. (US 6,763,228 B2). Prentice et al. teaches the precision automatic

gain control AGC for the <u>direct conversion of RF signals</u> [the zero intermediate frequency

ZIF transceiver 101 in Fig. 1, col. 7, lines 4-20, abstract], the gain control can be performed

in linear format, and also can be in <u>any desired format</u>, such as log format [col. 3, lines 30-

35].

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office

action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the

advisory action. In no event, however, will the statutory period for reply expire later than

SIX MONTHS from the date of this final action.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner

should be directed to Charles C. Chow whose telephone number is (571) 272-7889. The

examiner can normally be reached on 8:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor,

Edward Urban can be reached on (571) 272-7899. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status information

for unpublished applications is available through Private PAIR only. For more information

about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on

access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-

217-9197 (toll-free).

Charles Chow $\mathcal{C}.\mathcal{C}.$

June 17,2005.

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